Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **OUTPUT A**
2. **INPUT A-**
3. **INPUT A+**
4. **V-**
5. **INPUT B+**
6. **INPUT B-**
7. **OUTPUT B**
8. **V+**

**.104”**

**.059”**

**6 5 4 3**

**7 8 1 2**

**L**

**F**

**4**

**1**

**2**

**B**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V- or FLOATING**

**Mask Ref: LF412B**

**APPROVED BY: DK DIE SIZE .059” X .104” DATE: 12/12/16**

**MFG: NATIONAL THICKNESS .015” P/N: LF412A**

**DG 10.1.2**

#### Rev B, 7/19/02